Remarks/Arguments

Claim 13 has been cancelled.

Double Patenting

Claim 13 was objected to under 37 C.F.R. § 1.75 as being a substantial duplicate of claim 12. Accordingly, claim 13 has been cancelled.

Rejections under 35 U.S.C. § 102(b)

In the Office Action, claims 1-3, 11-17, and 21-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,246,083 to Wendell P. Noble (herein "*Noble*"). Applicants respectfully request reconsideration of this rejection for at least the following reasons.

In rejecting claim 1, the Examiner alleges that *Noble* discloses "a two-transistor DRAM cell (Figure 2) consisting: an NMOS device (26) with a first gate (65, column 6, lines 10-15); a PMOS device (28, column 6, lines 10-15) with a second gate; the PMOS device coupled to the NMOS device (Figure 2); and a storage node (110) coupled to the second gate (Figure 2, column 6, lines 20)." See Office Action, page 3. Applicants respectfully disagree with this interpretation of *Noble*. In particular, Applicants submit that *Noble* **does not** disclose a two-transistor DRAM cell having a *PMOS* device coupled to an NMOS device. Instead, *Noble* teaches a two-transistor gain cell (14) that includes a *p-channel JFET* (28) coupled to an NMOS device (26). See Figure 2, column 6, lines 10-15 of *Noble*. For at least this reason, claim 1 is not anticipated by *Noble*.

Furthermore, one skilled in the art would not be motivated to modify the teaching of *Noble* such that the p-channel JFET (28) of the two-transistor gain cell (14), as taught in *Noble*, is replaced with a PMOS device. That is, *Noble* **teaches away** from such modification since it teaches a specific two-transistor gain cell (14) **having a specific structure** that includes an NMOS device coupled to a *p-channel JFET* device. In particular, *Noble*, in column 6, lines 35-67, and column 7, lines 1-18, with reference to Figure 3, teaches a vertical gain cell 14 having a particular structure that includes a vertical write transistor (i.e., NMOS) 26 and a vertical read transistor (i.e., p-channel JFET) 28, coupled together in a particular structural manner as shown in Figure 3.

Noble further states in column 7, lines 6-18, the advantages of such a structure. Applicants submit that such advantages, as alleged in *Noble,* would not be realized if the p-channel JFET 28 as depicted in Figure 3 of *Noble* were to be replaced with a PMOS device. For at least the above reasons, claim 1 is patentable over *Noble*.

Independent claims 11 and 21 have similar features as claim 1 and is, therefore, likewise patentable over *Noble*. Claims 2-3, 12, 14-17, and 22-23 depend from and add additional features to independent claims 1, 11, and 21, respectively. Therefore, by virtue of their dependency, claims 2-3, 12, 14-17, and 22-23 are also patentable over *Noble*.

CONCLUSION

In view of the foregoing, the Applicants respectfully submit that claims 1-3, 11, 12, 14-17 and 21-23 are in condition for allowance. Thus, early issuance of Notice of Allowance is respectfully requested.

If the Examiner has any questions, he is invited to contact the undersigned at 503-796-2099.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,

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